Bandwidth Efficient Baseband Multi-Modulator

Wai Fong, Andrew Gray and Pen-Shu Yeh

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Program Objective

- Select a set of bandwidth efficient modulations from CCSDS *Radio Frequency (RF) and Modulation Systems* 401.0-B: Blue Book, Rec. 2.4.17A, 2.4.17B, and 2.4.18.
- Develop the high rate baseband multi-modulator (HRBM) on a flight applications specific integrated circuit (ASIC) for operational speeds >300 Mbps.
- Evaluate modulation designs with an FPGA implementation.
- Interface the HRBM with the RF modulator provided by the Solar Dynamics Observer (SDO) project.
- Test the entire modulator on the TDRSS Ka-band 650 MHZ service.

Background

- Space Frequency Coordination Group (SFCG) approved an RF mask recommendation 17-2 in 1998, last revision 21-2 in 2002.
- SFCG rec. 17-2/21-2 becomes NASA policy for missions to meet.
- CCSDS Rec. 2.4.17A, 2.4.17B, and 2.4.18, approved 2001, contains specifications for Offset Quadrature Shift Keying (OQPSK)-type modulations: Gaussian Minimum Shift Keying (GMSK), Filtered-OQPSK, Shaped-OQPSK (S-OQPSK), Feher QPSK-Type B (FQPSK-B) and also higher-order coded modulations, i.e. 8-PSK TCM at 2.0, 2.25, 2.5, and 2.75 bits/symbol/Hz.
- These modulations all conform to the SFCG mask.

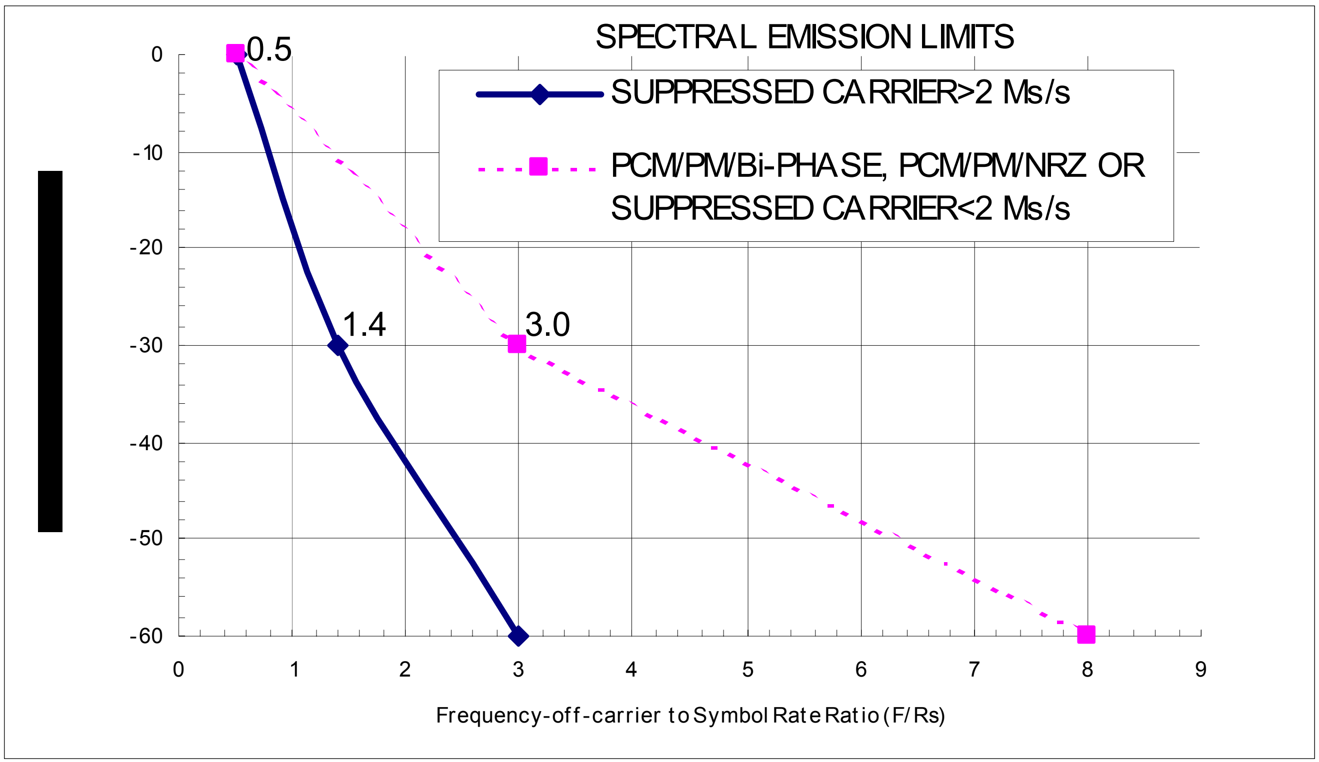
Overview of Requirements

- Develop HRBM chip and board for realizing bandwidth efficient modulations
  - A path to flight realization
    - Re-usable implementation: HDL implementation will be used for ASIC design
    - Final implementation in radiation tolerant ASIC
  - Reduce risk of the ASIC realization of the three modulations
    - Verify modulation performance for the three modulations in laboratory and field environments
      - Spectrum, RF Interface, others
  - Implement a suite of CCSDS recommended modulations
    - Requirements include meeting spectral performance determined theoretically and with computer simulation **within practical limits**
    - Hard requirement for the spectrum of the modulator in all modes is to meet CCSDS spectral mask

Modulation Selection

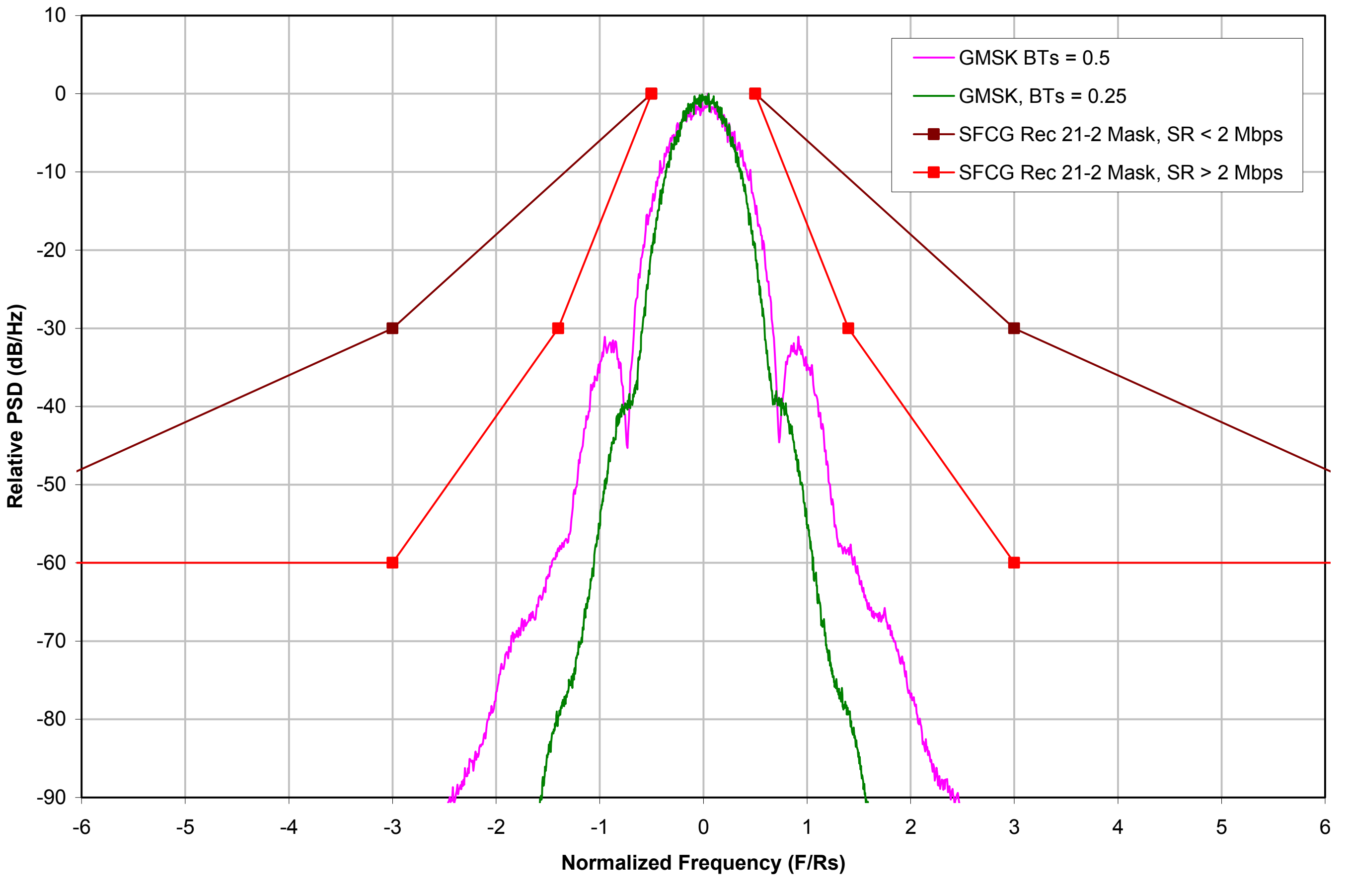
- Three CCSDS modulations were selected for HRBM implemention.
  - GMSK due to it's excellent sideband suppression, receiver availability and BER performance with a Viterbi receiver.
  - Filtered-OQPSK due to it's filter flexibility and ability to accommodate independent channels.
  - 8-PSK TCM due to it's higher order modulation can produce more bandwidth efficiency.
- Two modulations were not selected.
  - FQPSK-B was not selected because it's spectra performance was not better than GMSK and it has a quasi-constant envelope signal.
  - S-OQPSK was not selected because of time constraint and complexity (although it has marginally the best spectra performance.)

SFCG MASK

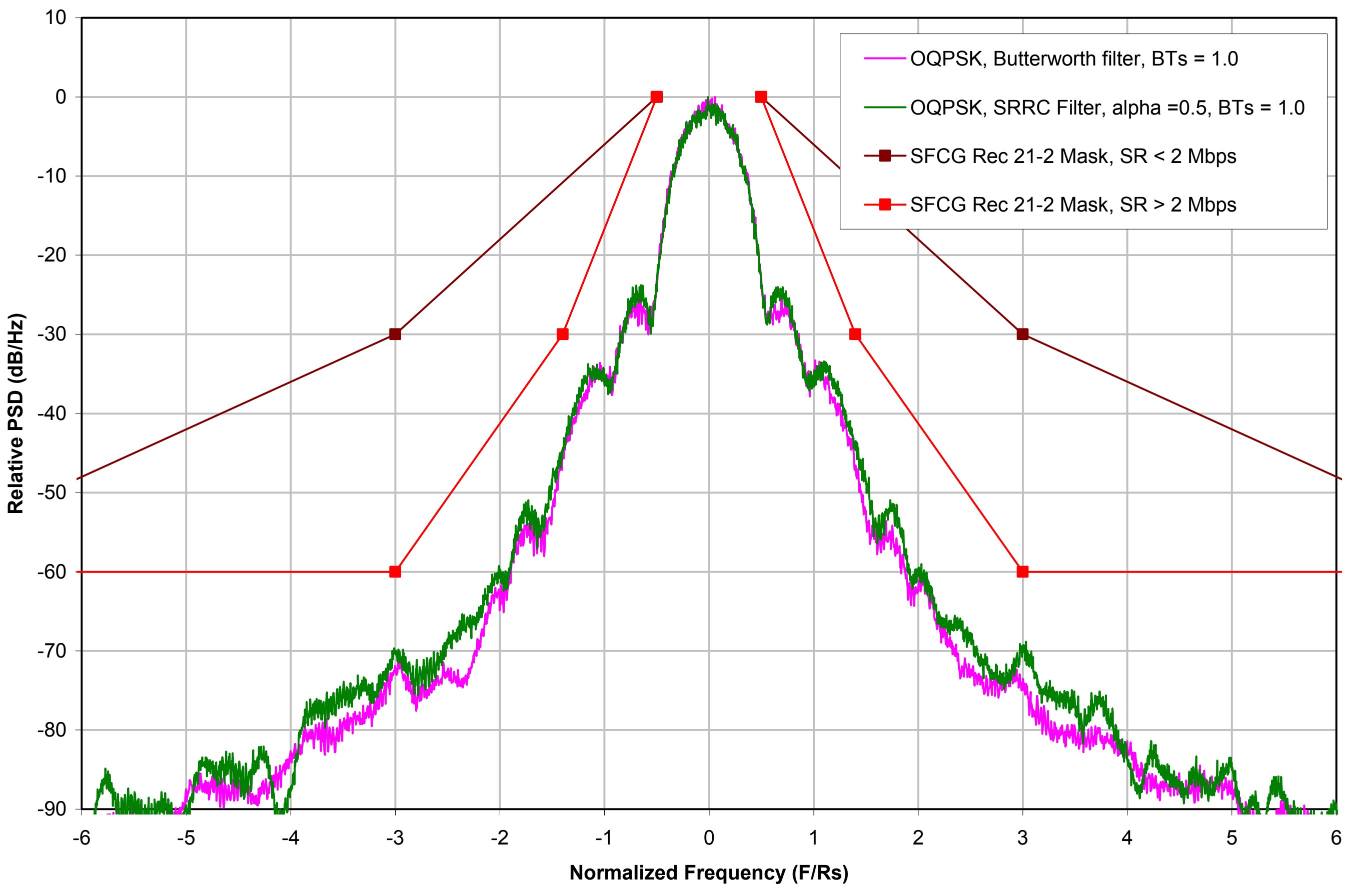


SPECTRAL EMISSION LIMITS
SUPPRESSED CARRIER>2 Ms/s
PCM/PM/Bi-PHASE, PCM/PM/NRZ OR SUPPRESSED CARRIER<2 Ms/s
[redacted]
0
-10
-20
-30
-40
-50
-60
0.5
1.4
3.0
0
1
2
3
4
5
6
7
8
9
Frequency-off-carrier to Symbol Rate Ratio (F/Rs)

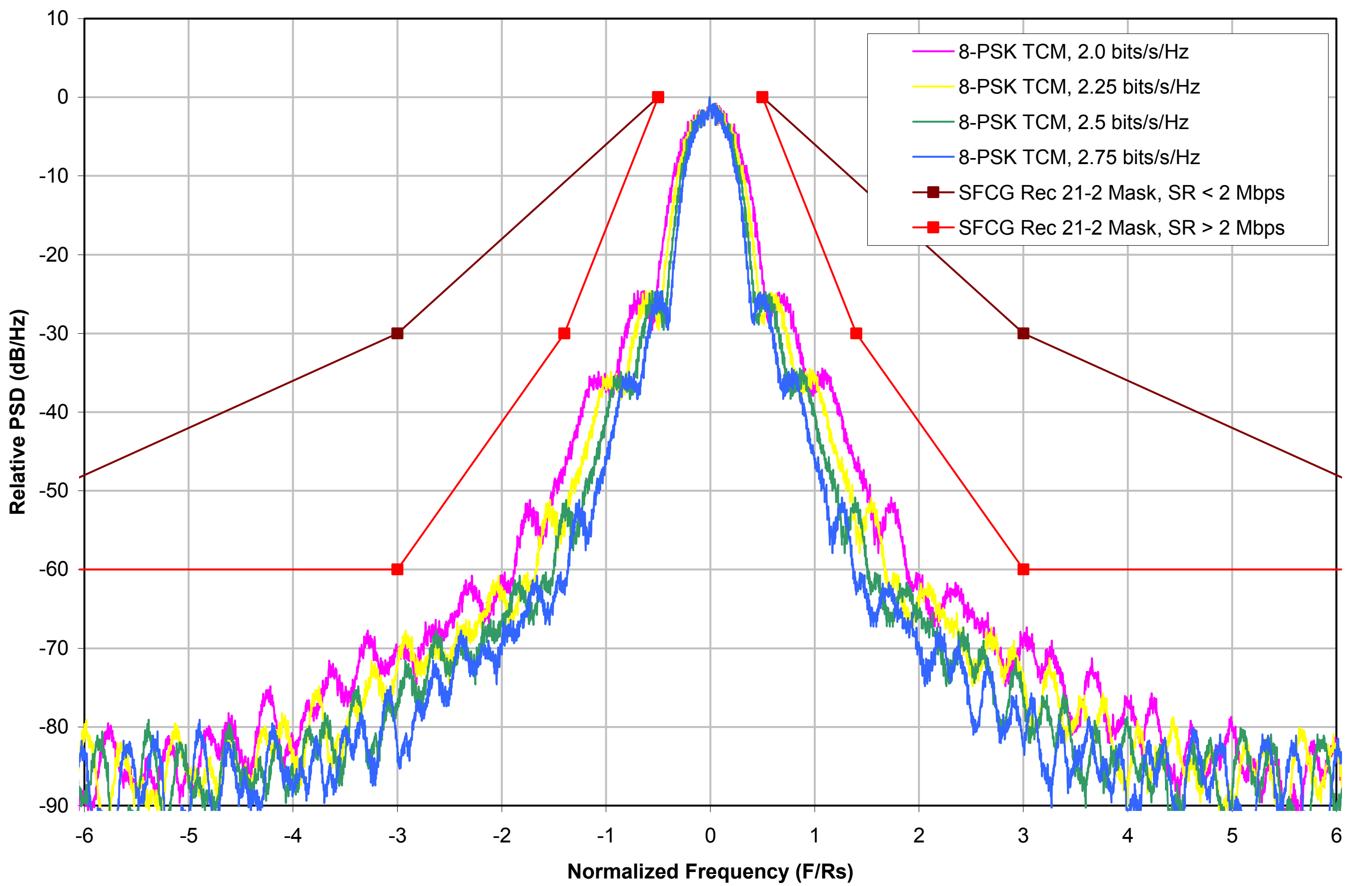
GMSK Spectra



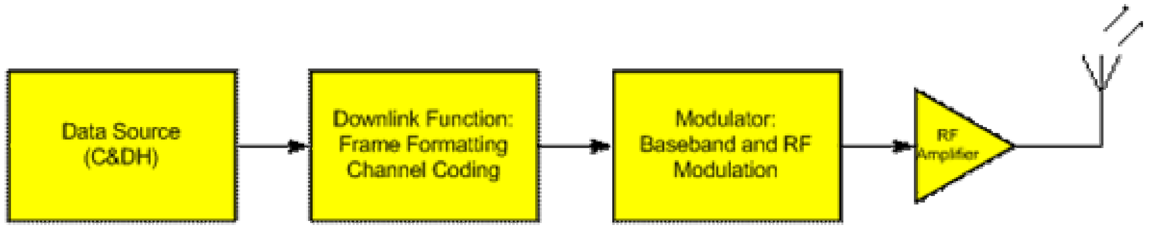
Filtered OQPSK Spectra



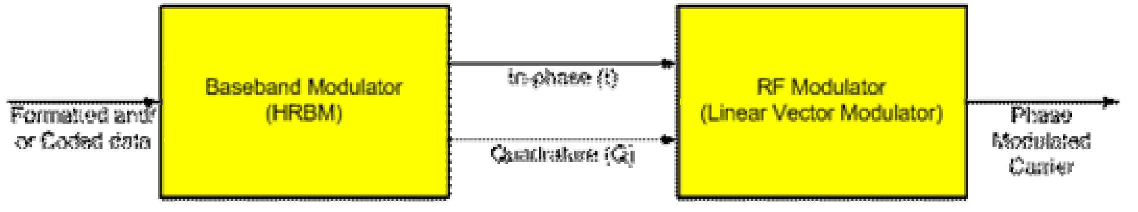
8-PSK TCM Spectra



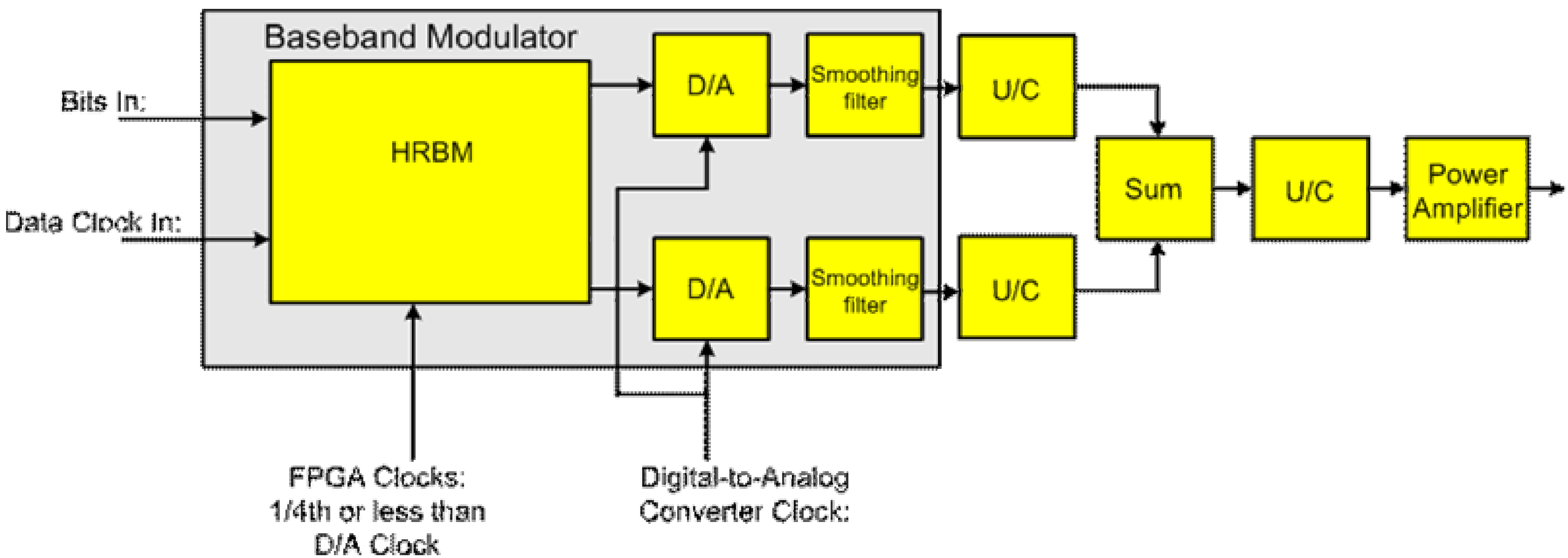
Spacecraft Downlink Communication Block Diagram



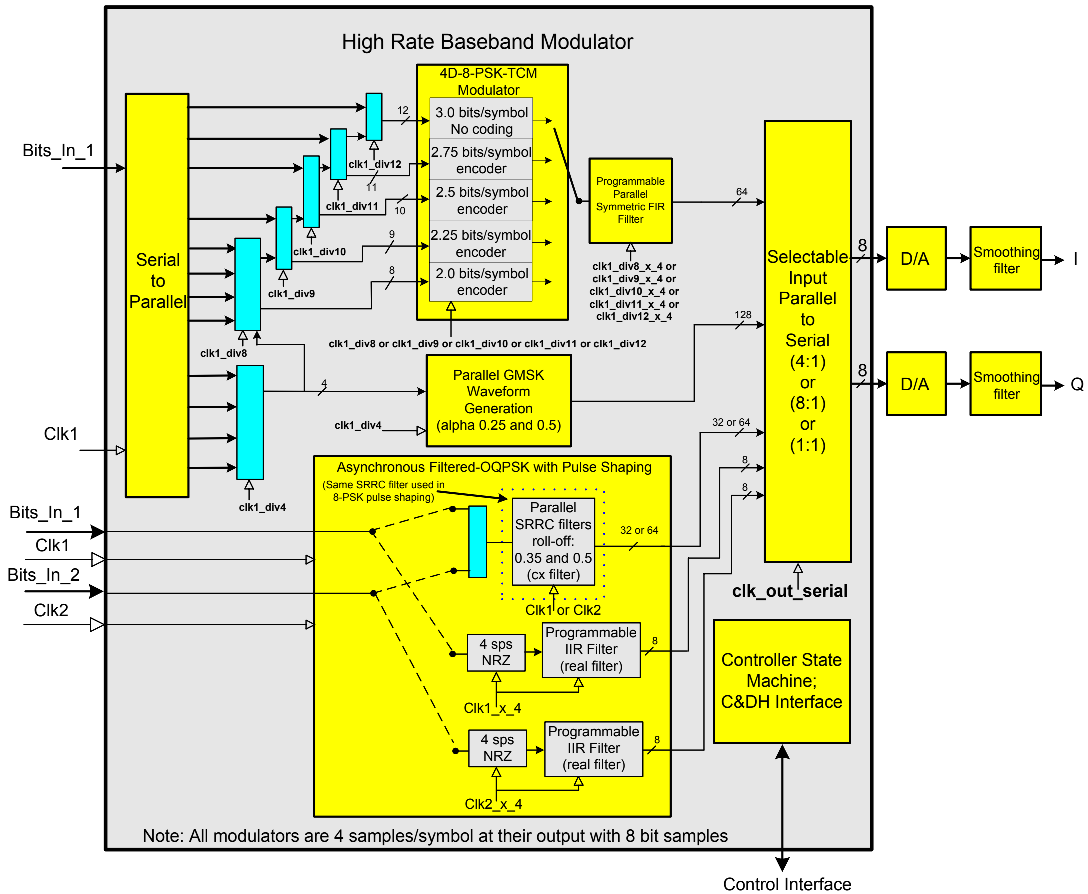
Modulator Block Diagram



Modulator Detailed Block Diagram

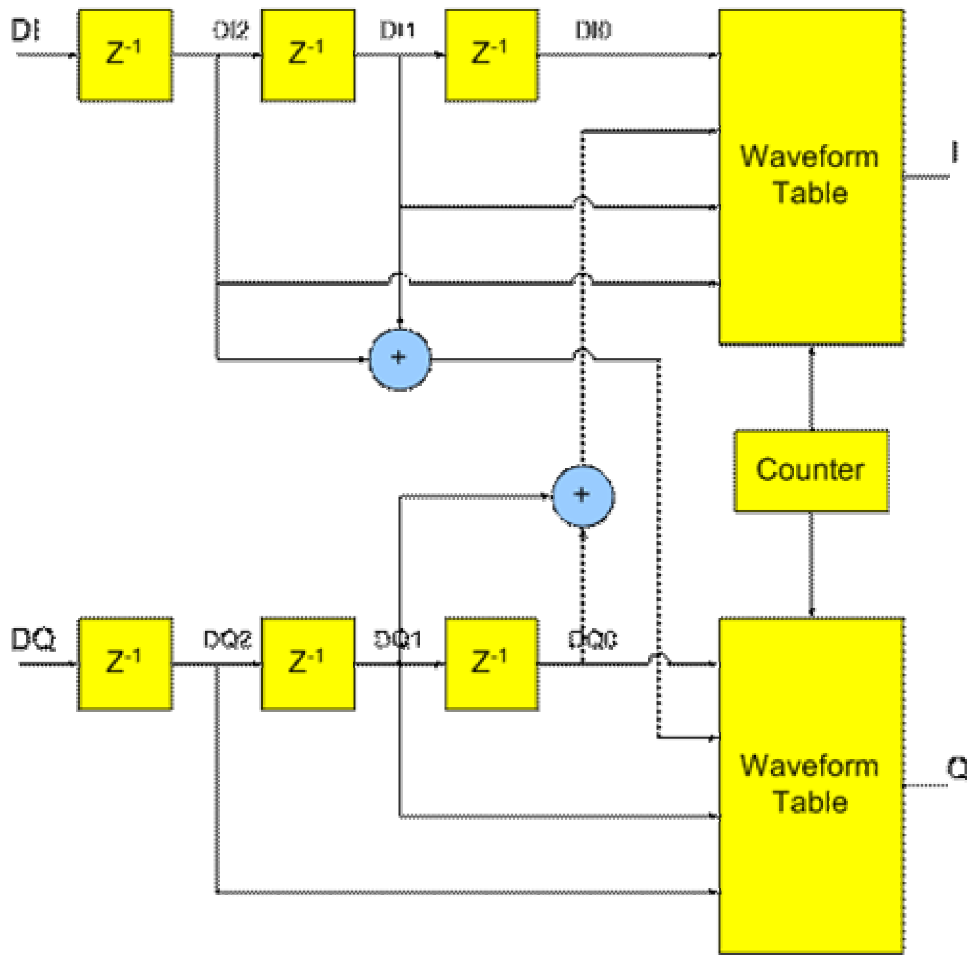


Baseband Modulator Block Diagram

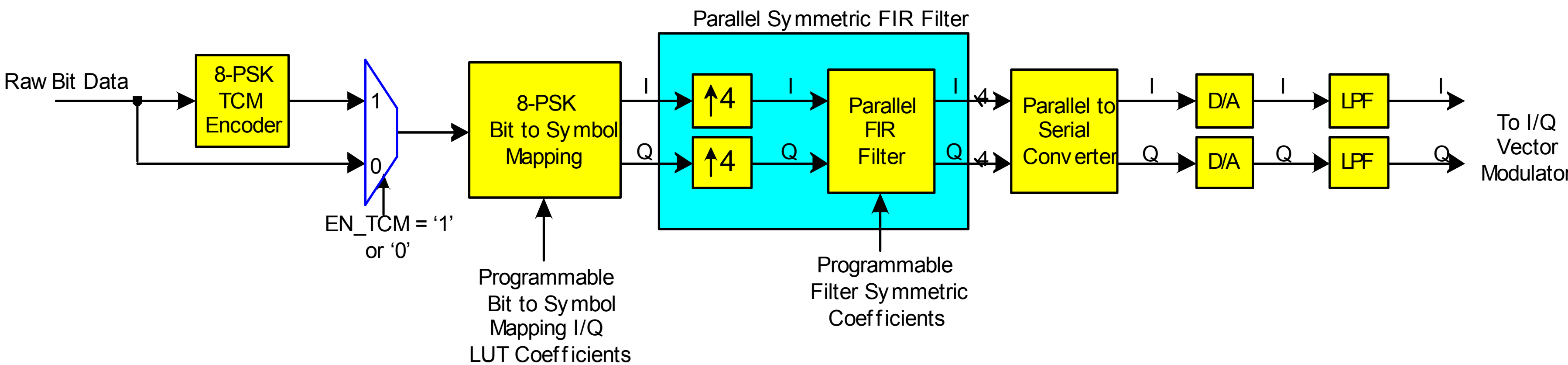


GMSK Architecture

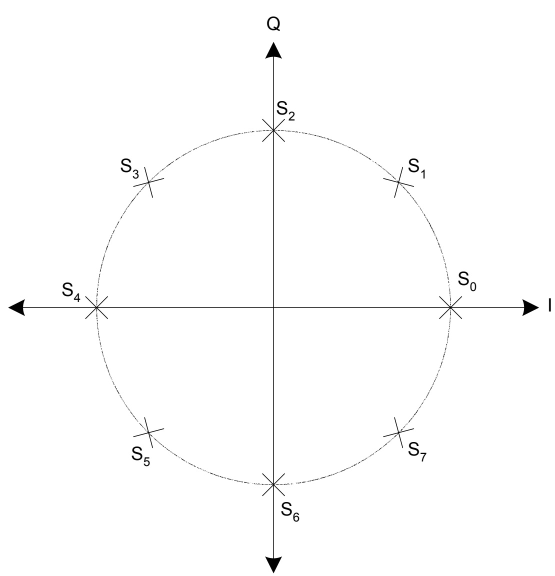
- GMSK baseband modulators generate GMSK coding/pulse shaping primarily via wavelet look-up tables

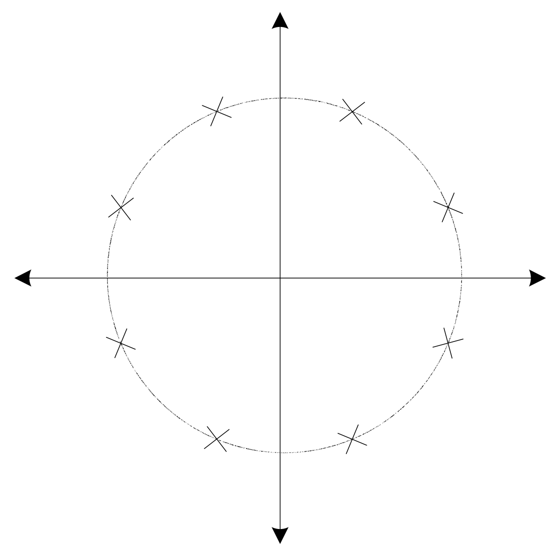


8-PSK TCM Architectures

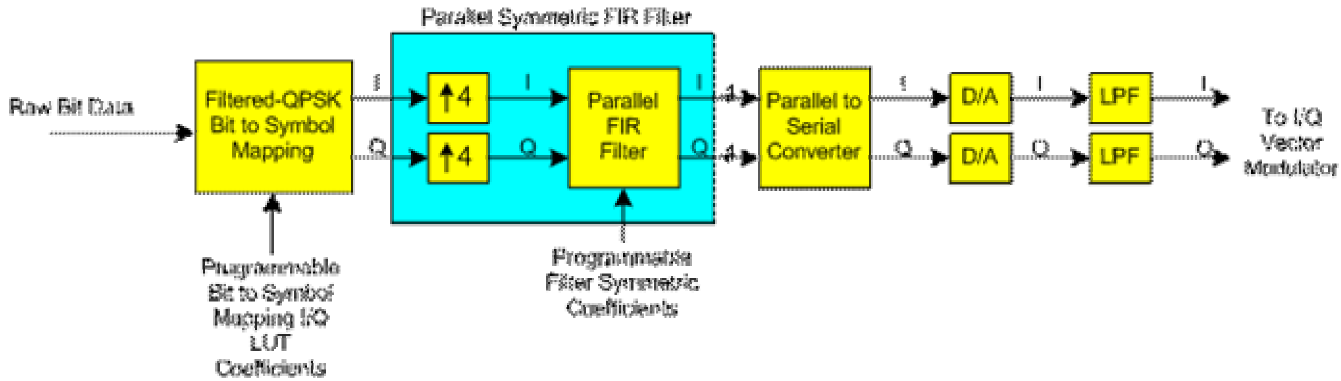


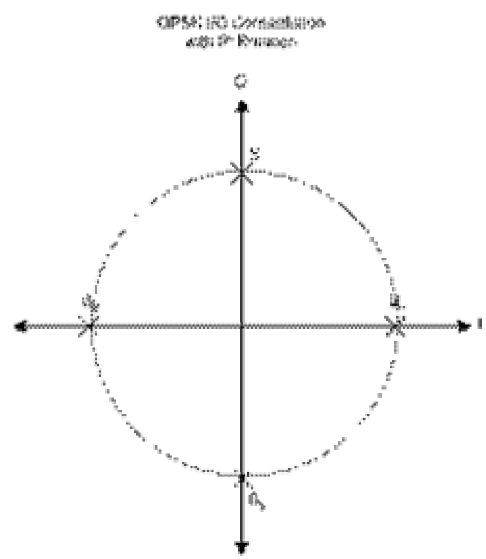
8-PSK I/Q Constellation with 0° Rotation

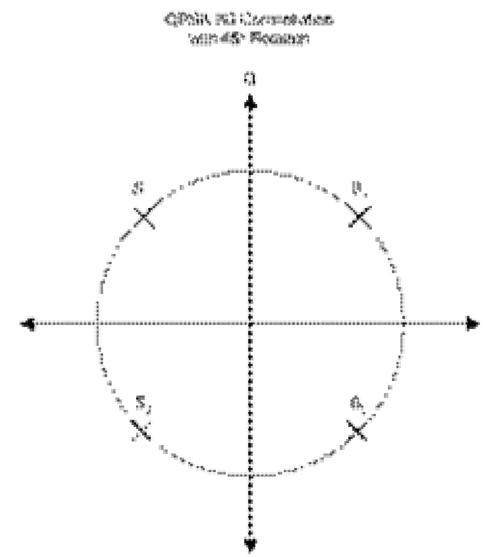




Filtered-OQPSK Architecture





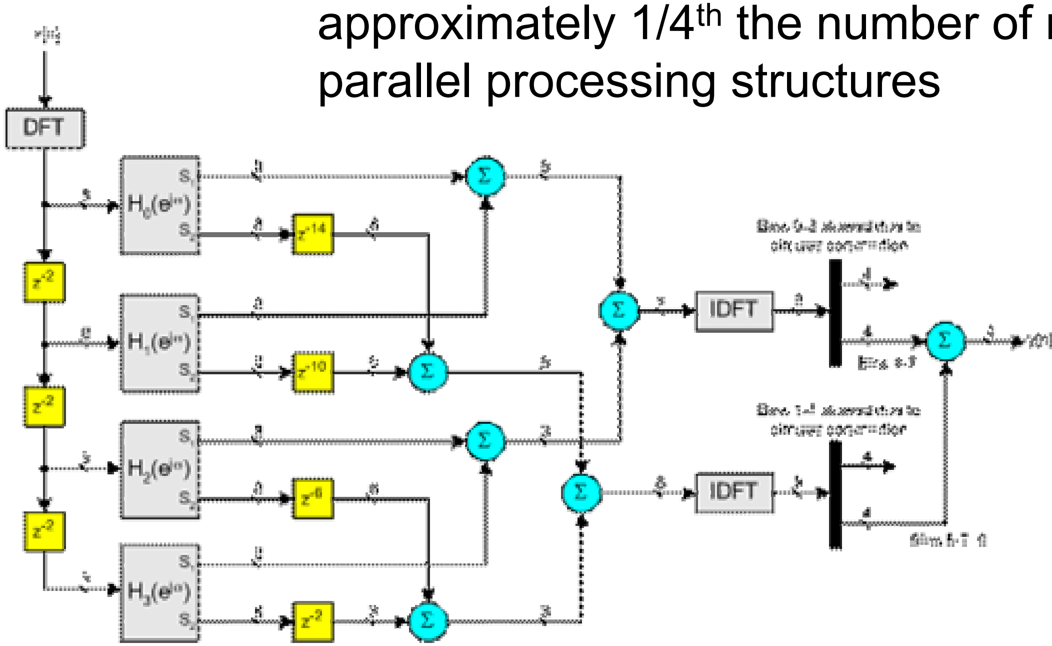


FIR Filter Design Considerations

- Size of the design is dominated by FIR filter.
- Number of taps drive the complexity and size of FIR filter.
- Simulations performed to trade-off number of taps vs. out-of-band spectral response.
- Perform end-to-end simulations to confirm performance.
- 64 taps is the best trade-off number giving good BER performance, meeting the SFCG mask and reducing the complexity as much as possible.

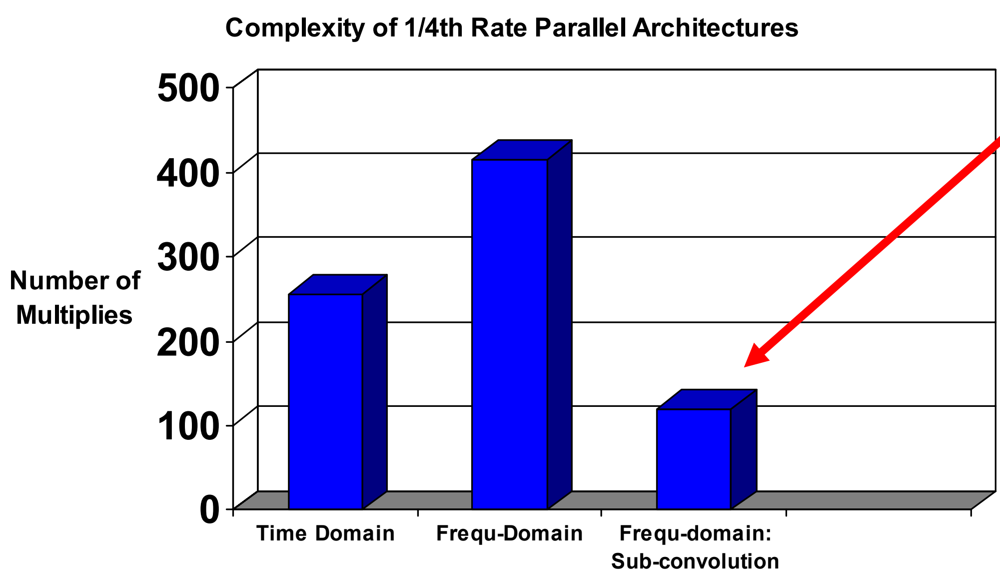
FIR Filter Architecture

- Finite Impulse Response Pulse-Shaping Structure
  - 64 Coefficients
  - Programmable coefficients
  - Parallel Implementation
    - Processing rate is approximately 1/4th symbol rate or 1/12th the bit rate (no coding)
  - Frequency Domain Implementation for Reduced Complexity
    - Novel parallel frequency domain structure results in approximately 1/4th the number of multipliers of other parallel processing structures



FIR Filter Complexity

- Frequency domain implementation employing sub-convolution for reduced complexity
  - 64 coefficient square root raised cosine pulse-shaping filter
    - Symmetric finite impulse response (FIR): a time domain approach requires 32 multiplies with the use of additional (32) tap delay lines
    - Require a minimum of 1/4th clock rate reduction; parallelization of at lest 4
    - Require two SRRC filters; one for I channel and one for Q channel

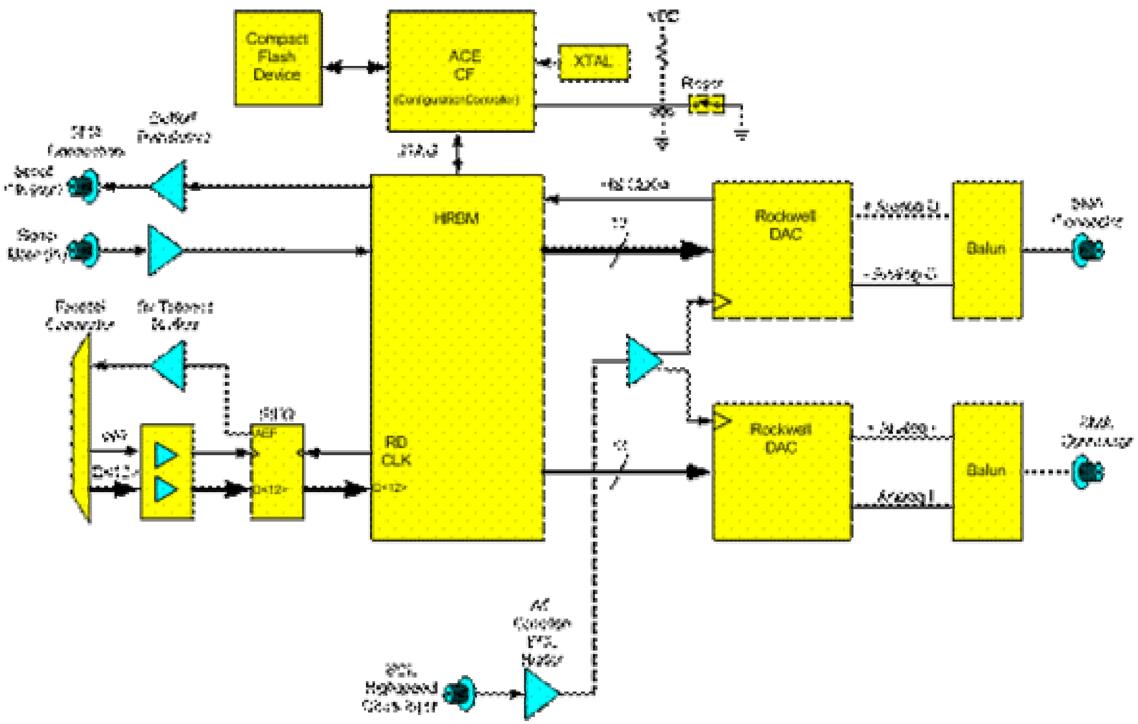


•FPGA prototype would not be feasible without this reduced complexity architecture developed under this task (a multiple FPGA solution would be required)
•This innovation resulted in a patent application, NASA Tech Brief and is being published in the IEEE ISCAS 2003

End-to-End Simulation Results

- Filtered-OQPSK with 64 tap SRRC (alpha=0.5) filtering with AWGN and no distortions:
  - 1 dB implementation loss (w.r.t. ideal QPSK) and Integrate and dump (I/D) receiver.
  - 0 dB imp. loss with a matched filter (MF) receiver
- Filtered-OQPSK with 64 tap SRRC (alpha=0.5) filtering through ESA SSPA with AWGN and TDRSS Ka-band service at 300Mbps:
  - 1.4 dB loss with MF receiver
  - 1.5 dB loss with I/D receiver
- Filtered-OQPSK with 64 tap SRRC (alpha=0.5) filtering through ESA SSPA with AWGN and TDRSS Ku-band service at 300Mbps:
  - 2.0 dB loss with MF receiver
  - 3.0 dB loss with I/D receiver

FPGA Board Block Diagram



Status

- There are two development tracks: 1. flight ASIC modulator along with the ASIC demodulator/decoder and 2. the FPGA modulator.
- Currently, 8-PSK TCM have been verified and translated into a Xilinx FPGA.
- The FPGA FIR filter design has been simulated to 100 MHz operation. This corresponds to an input date rate of 300 Mbps with Filtered 8-PSK.
- The FPGA prototype board design is complete will be submitted for fabrication this week.
- By September 2003, this board should be completely checked out.
- The ASIC design has started and is currently undergoing an architectural study.
- After this is competed, a detail design should start sometime in September 2003.
- Then a fabrication run would be initiated by the fourth quarter 2003 with the chips delivered in the first quarter 2004.